TUSB2046B-Q1 4-Port HUB for the Universal Serial BUS With Optional Serial EEPROM Interface

1 Features

- Qualified for Automotive Applications
- Fully Compliant With the USB Specification as a Full-Speed Hub: TID #30220231
- 32-Pin VQFN Package With a 0.5-mm Pitch
- 3.3-V Low-Power ASIC Logic
- Integrated USB Transceivers
- State Machine Implementation Requires No Firmware Programming
- One Upstream Port and Four Downstream Ports
- All Downstream Ports Support Full-Speed and Low-Speed Operations
- Two Power-Source Modes
  - Self-Powered Mode
  - Bus-Powered Mode
- Power Switching and Overcurrent Reporting Is Provided Ganged or Per Port
- Supports Suspend and Resume Operations
- Supports Programmable Vendor ID and Product ID With External Serial EEPROM
- 3-State EEPROM Interface Allows EEPROM Sharing
- Push-Pull Outputs for $\overline{\text{PWRON}}$ Eliminate the Need for External Pullup Resistors
- Noise Filtering on $\overline{\text{OVRCUR}}$ Provides Immunity to Voltage Spikes
- Package Pinout Allows Two-Layer PCB
- Low EMI Emission Achieved by a 6-MHz Crystal Input
- Migrated From Proven TUSB2040 Hub
- Lower Cost Than the TUSB2040 Hub
- Enhanced System ESD Performance
- Supports 6-MHz Operation Through a Crystal Input or a 48-MHz Input Clock
- No Special Driver Requirements; Works Seamlessly With Any System Having USB Stack Support

2 Applications

- Automotive Infotainment

3 Description

The TUSB2046B-Q1 is a 3.3-V CMOS hub device that provides one upstream port and four downstream ports in compliance with the Universal Serial Bus (USB) specification as a full-speed hub. Because this device is implemented with a digital state machine instead of a microcontroller, no firmware programming is required. Fully-compliant USB transceivers are integrated into the ASIC for all upstream and downstream ports. The downstream ports support both full-speed and low-speed devices by automatically setting the slew rate according to the speed of the device attached to the ports. The configuration of the BUSPWR pin selects either the bus-powered or the self-powered mode.

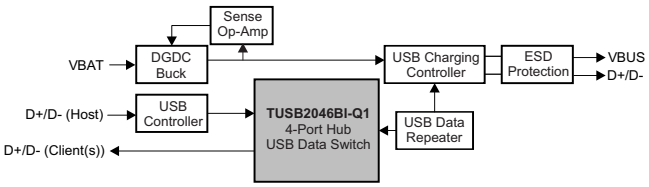
Configuring the GANGED input determines the power-switching and overcurrent-detection modes for the downstream ports. External power-management devices, such as the TPS2044, are required to control the 5-V source to the downstream ports according to the corresponding value of the $\overline{\text{PWRON}}$ pin. On detecting any overcurrent conditions, the power-management device sets the corresponding $\overline{\text{OVRCUR}}$ pin of the TUSB2046B-Q1 to a logic low. If GANGED is high, all $\overline{\text{PWRON}}$ outputs switch together, and if any $\overline{\text{OVRCUR}}$ is activated, all ports transition to the power-off state. If GANGED is low, the $\overline{\text{PWRON}}$ outputs and $\overline{\text{OVRCUR}}$ inputs operate on a per-port basis.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TUSB2046B-Q1	VQFN (32)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Key Graphic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2013) to Revision A	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Changed part number here and throughout the text and illustrations of the data sheet from TUSB2046B to TUSB2046BI-Q1	1
• Deleted VF Package pinout drawing	4
• Revised pinout drawing	4

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5 Description (Continued)

The TUSB2046B-Q1 provides the flexibility of using a 6-MHz or a 48-MHz clock. The logic level of the TSTMODE pin controls the selection of the clock source. When TSTMODE is low, the output of the internal APLL circuitry is selected to drive the internal core of the device. When TSTMODE is high, the TSTPLL/48MCLK input is selected as the input clock source and the APLL circuitry is powered down and bypassed. The internal oscillator cell is also powered down while TSTMODE is high.

Low EMI emission is achieved because the TUSB2046B-Q1 is able to use a 6-MHz crystal input. Connect the crystal as shown in Figure 8. An internal PLL then generates the 48-MHz clock used to sample data from the upstream port and to synchronize the 12 MHz used for the USB clock. If low-power suspend and resume are desired, a passive crystal or resonator must be used. However, a 6-MHz oscillator may be used by connecting the output to the XTAL1 pin and leaving the XTAL2 pin open. The oscillator TTL output must not exceed 3.6 V.

For 48-MHz operation, the clock cannot be generated with a crystal using the XTAL2 output because the internal oscillator cell supports only the fundamental frequency.

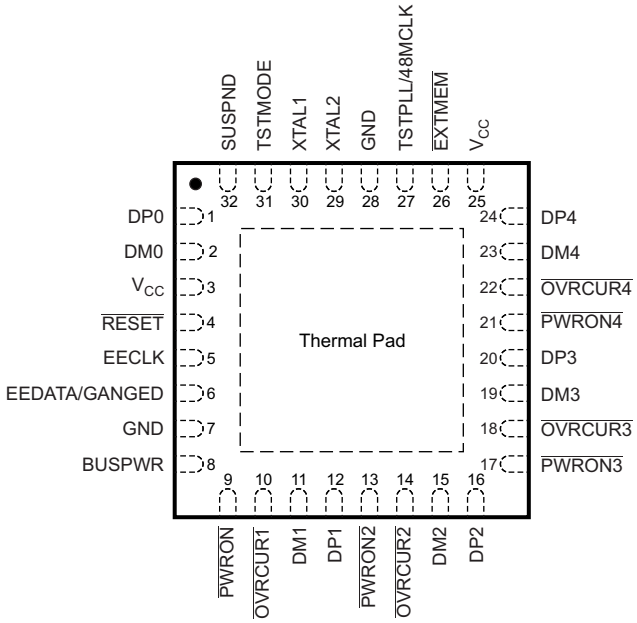
See Figure 7 and Figure 9 in the *input clock configuration* section for more-detailed information regarding the input clock configuration.

The $\overline{\text{EXTMEM}}$ pin enables or disables the optional EEPROM interface. When the $\overline{\text{EXTMEM}}$ pin is high, the product ID (PID) displayed during enumeration is the general-purpose USB hub. For this default, pin 5 is disabled and pin 6 functions as the GANGED input pin. If custom PID and vendor ID (VID) descriptors are desired, the $\overline{\text{EXTMEM}}$ pin must be low ($\overline{\text{EXTMEM}}$ = 0). For this configuration, pin 5 and pin 6 function as the EEPROM interface with pin 5 and pin 6 functioning as EECLK and EEDATA, respectively. See Table 1 for a description of the EEPROM memory map.

Other useful features of the TUSB2046B-Q1 include a package with a 0.8-mm pin pitch for easy PCB routing and assembly, push-pull outputs for the $\overline{\text{PWRON}}$ pins to eliminate the need for pullup resistors required by traditional open-collector I/Os, and $\overline{\text{OVRCUR}}$ pins having noise filtering for increased immunity to voltage spikes.

6 Pin Configuration and Functions

RHB Package
32-Pin VQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BUSPWR	8	I	Power source indicator. BUSPWR is an active-high input that indicates whether the downstream ports source their power from the USB cable or a local power supply. For the bus-power mode, this pin must be pulled to 3.3 V, and for the self-powered mode, this pin must be pulled low. Input must not change dynamically during operation.
DM0	2	I/O	Root port USB differential data minus. DM0 paired with DP0 constitutes the upstream USB port.
DM1	11	I/O	USB differential data minus. DM1–DM4 paired with DP1–DP4 support up to four downstream USB ports.
DM2	15		
DM3	19		
DM4	23		
DP0	1	I/O	Root port USB differential data plus. DP0 paired with DM0 constitutes the upstream USB port.
DP1	12	I/O	USB differential data plus. DP1–DP4 paired with DM1–DM4 support up to four downstream USB ports.
DP2	16		
DP3	20		
DP4	24		
EECLK	5	O	EEPROM serial clock. When $\overline{\text{EXTMEM}}$ is high, the EEPROM interface is disabled. The EECLK pin is disabled and must be left floating (unconnected). When $\overline{\text{EXTMEM}}$ is low, EECLK acts as a 3-state serial clock output to the EEPROM with a 100-µA internal pulldown.
EEDATA/ GANGED	6	I/O	EEPROM serial data- and power-management mode indicator. When $\overline{\text{EXTMEM}}$ is high, EEDATA/GANGED selects between ganged or per-port power overcurrent detection for the downstream ports. When $\overline{\text{EXTMEM}}$ is low, EEDATA/GANGED acts as a serial data I/O for the EEPROM and is internally pulled down with a 100-µA pulldown. This standard TTL input must not change dynamically during operation.
$\overline{\text{EXTMEM}}$	26	I	When $\overline{\text{EXTMEM}}$ is high, the serial EEPROM interface of the device is disabled. When $\overline{\text{EXTMEM}}$ is low, pins 5 and 6 are configured as the clock and data pins of the serial EEPROM interface, respectively.
GND	7, 28		GND pins must be tied to ground for proper operation.

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{\text{OVRCUR1}}$	10	I	Overcurrent input. $\overline{\text{OVRCUR1}}$–$\overline{\text{OVRCUR4}}$ are active-low. For per-port overcurrent detection, one overcurrent input is available for each of the four downstream ports. In the ganged mode, any $\overline{\text{OVRCUR}}$ input may be used and all $\overline{\text{OVRCUR}}$ pins must be tied together. $\overline{\text{OVRCUR}}$ pins are active-low inputs with noise-filtering logic.
$\overline{\text{OVRCUR2}}$	14		
$\overline{\text{OVRCUR3}}$	18		
$\overline{\text{OVRCUR4}}$	22		
$\overline{\text{PWRON1}}$	9	O	Power-on and -off control signals. $\overline{\text{PWRON1}}$–$\overline{\text{PWRON4}}$ are active-low, push-pull outputs. Push-pull outputs eliminate the pullup resistors which open-drain outputs require. However, the external power switches that connect to these pins must be able to operate with 3.3-V inputs because these outputs cannot drive 5-V signals.
$\overline{\text{PWRON2}}$	13		
$\overline{\text{PWRON3}}$	17		
$\overline{\text{PWRON4}}$	21		
$\overline{\text{RESET}}$	4	I	$\overline{\text{RESET}}$ is an active-low TTL input with hysteresis and must be asserted at power up. When $\overline{\text{RESET}}$ is asserted, all logic is initialized. Generally, a reset with a pulse duration between 100 µs and 1 ms is recommended after 3.3-V V_{CC} reaches 90% of its full value. The clock signal must be active during the last 60 µs of the reset window.
SUSPND	32	O	Suspend status. SUSPND is an active-high output available for external logic power-down operations. During the suspend mode, SUSPND is high. SUSPND is low for normal operation.
TSTMODE	31	I	Test or mode pin. TSTMODE is used as a test pin during production testing. This pin must be tied to ground or 3.3-V V_{CC} for normal 6-MHz or 48-MHz operation, respectively.
TSTPLL/ 48MCLK	27	I/O	Test or 48-MHz clock input. TSTPLL/48MCLK is used as a test pin during production testing. This pin must be tied to ground for normal 6-MHz operation. If 48-MHz input clock is desired, a 48-MHz clock source (no crystal) can be connected to this input pin.
V_{CC}	3, 25		3.3-V supply voltage
XTAL1	30	I	Crystal 1. XTAL1 is a 6-MHz crystal input with 50% duty cycle. An internal PLL generates the 48-MHz and 12-MHz clocks used internally by the ASIC logic.
XTAL2	29	O	Crystal 2. XTAL2 is a 6-MHz crystal output. This pin must be left open when using an oscillator.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage[2]		–0.5	3.6	V
V_I	Input voltage		–0.5	V_{CC} + 0.5	V
V_O	Output voltage		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0 V or V_I < V_{CC}		±20	mA
I_{OK}	Output clamp current	V_O < 0 V or V_O < V_{CC}		±20	mA
T_A	Operating free-air temperature		–40	85	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage levels are with respect to GND.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	±3000	V
		Charged device model (CDM), per AEC Q100-011	±2000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3.3		3.6	V
V_I	Input voltage, TTL or LVCMOS	0		V_{CC}	V
V_O	Output voltage, TTL or LVCMOS	0		V_{CC}	V
$V_{IH(REC)}$	High-level input voltage, signal-ended receiver	2		V_{CC}	V
$V_{IL(REC)}$	Low-level input voltage, signal-ended receiver			0.8	V
$V_{IH(TTL)}$	High-level input voltage, TTL or LVCMOS	2		V_{CC}	V
$V_{IL(TTL)}$	Low-level input voltage, TTL or LVCMOS	0		0.8	V
$R_{(DRV)}$	External series differential-driver resistor	22 (–5%)		22 (5%)	Ω
$f_{(OPRH)}$	Operating (dc differential driver) high-speed mode			12	Mb/s
$f_{(OPRL)}$	Operating (dc differential driver) low-speed mode			1.5	Mb/s
V_{ICR}	Common-mode input-range differential receiver	0.8		2.5	V
t_t	Input transition times, TTL or LVCMOS	0		25	ns
T_J	Junction temperature range	–40		115	°C
T_A	Operating free-air temperature	–40		85	°C

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7.4 Thermal Information

THERMAL METRIC[1]		TUSB2046B-Q1 RHB (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	TTL or LVCMOS	I_{OH} = –4 mA	V_{CC} – 0.5			V
		USB data lines	$R_{(DRV)}$ = 15 kΩ to GND	2.8			
			I_{OH} = –12 mA (without $R_{(DRV)}$)	V_{CC} – 0.5			
V_{OL}	Low-level output voltage	TTL or LVCMOS	I_{OL} = 4 mA			0.5	V
		USB data lines	$R_{(DRV)}$ = 1.5 kΩ to 3.6 V			0.3	
			I_{OL} = 12 mA (without $R_{(DRV)}$)			0.5	
V_{IT+}	Positive input threshold	TTL or LVCMOS				1.8	V
		Single-ended	0.8 V ≤ V_{ICR} ≤ 2.5 V			1.8	
V_{IT-}	Negative-input threshold	TTL or LVCMOS		0.8			V
		Single-ended	0.8 V ≤ V_{ICR} ≤ 2.5 V	1			
V_{hys}	Input hysteresis[1] ($V_{T+} – V_{T-}$)	TTL or LVCMOS		0.3		0.7	mV
		Single-ended	0.8 V ≤ V_{ICR} ≤ 2.5 V	300		500	
I_{OZ}	High-impedance output current	TTL or LVCMOS	V = V_{CC} or GND[2]			±10	µA
		USB data lines	0 V ≤ V_O ≤ V_{CC}			±10	
I_{IL}	Low-level input current	TTL or LVCMOS	V_I = GND			–1	µA
I_{IH}	High-level input current	TTL or LVCMOS	V_I = V_{CC}			1	µA
$z_{0(DRV)}$	Driver output impedance[3]	USB data lines	Static V_{OH} or V_{OL}	7.1		19.9	Ω
V_{ID}	Differential input voltage	USB data lines	0.8 V ≤ V_{ICR} ≤ 2.5 V	0.2			V
I_{CC}	Input supply current		Normal operation			40	mA
			Suspend mode			1	µA

(1) Applies for input buffers with hysteresis.
(2) Applies for open-drain buffers.
(3) Characterization only. Limits are approved by design and are not production tested.

7.6 Differential Driver Switching Characteristics Full-Speed Mode

over recommended ranges of operating free-air temperature and supply voltage, C_L = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Transition rise time for DP or DM	See Figure 1 and Figure 2	4		20	ns
t_f	Transition fall time for DP or DM	See Figure 1 and Figure 2	4		20	ns
$t_{(RFM)}$	Rise and fall time matching (1)	$(t_r / t_f) \times 100$	90%		110%	
$V_{O(CRS)}$	Signal crossover output voltage (1)		1.3		2	V

(1) Characterization only. Limits are approved by design and are not production tested.

7.7 Differential Driver Switching Characteristics Low Speed Mode

over recommended ranges of operating free-air temperature and supply voltage, C_L = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Transition rise time for DP or DM (1)	C_L = 200 pF to 600 pF, see Figure 1 and Figure 2	75		300	ns
t_f	Transition fall time for DP or DM (1)	C_L = 200 pF to 600 pF, see Figure 1 and Figure 2	75		300	ns
$t_{(RFM)}$	Rise and fall time matching (1)	$(t_r / t_f) \times 100$	80%		120%	
$V_{O(CRS)}$	Signal crossover output voltage (1)	C_L = 200 pF to 600 pF	1.3		2	V

(1) Characterization only. Limits are approved by design and are not production tested.

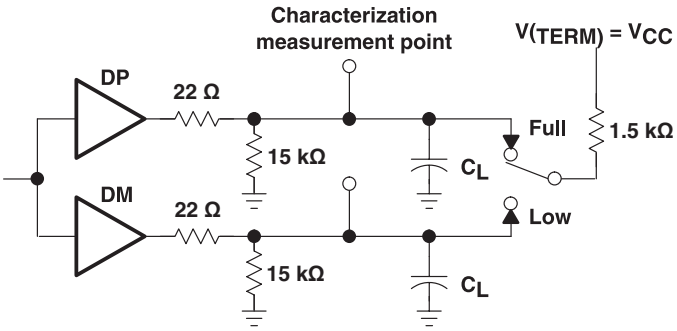
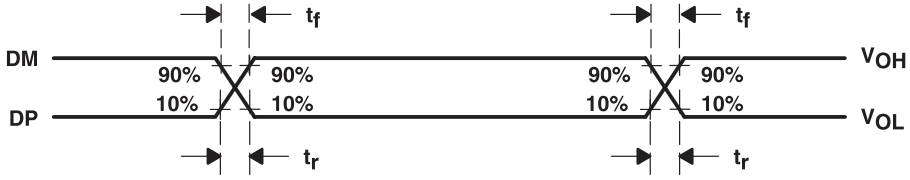


Figure 1. Differential Driver Switching Load



NOTE: The t_r/t_f ratio is measured as $t_{r(DP)}/t_{f(DM)}$ and $t_{r(DM)}/t_{f(DP)}$ at each crossover point.

Figure 2. Differential Driver Timing Waveforms

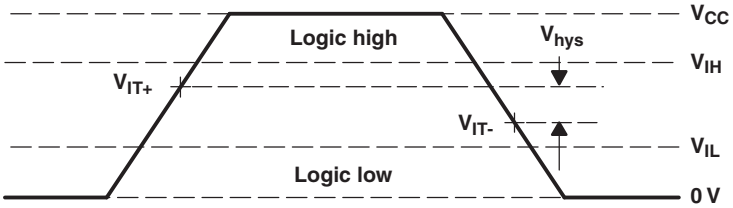


Figure 3. Single-Ended Receiver Input-Signal Parameter Definitions

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7.8 Typical Characteristics

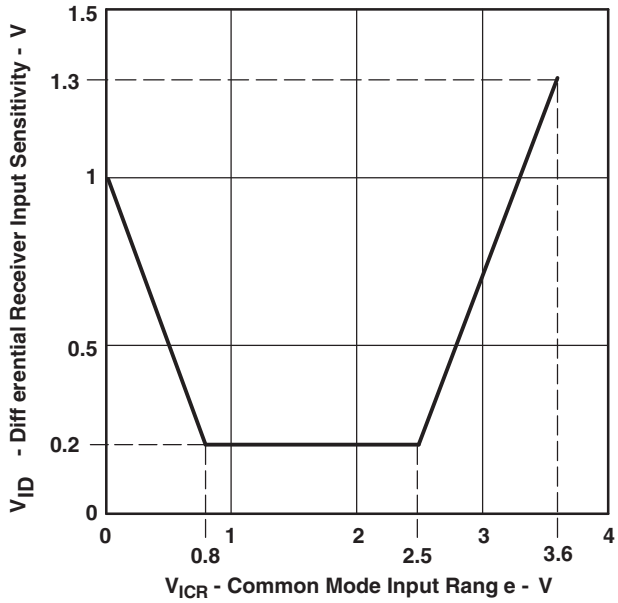


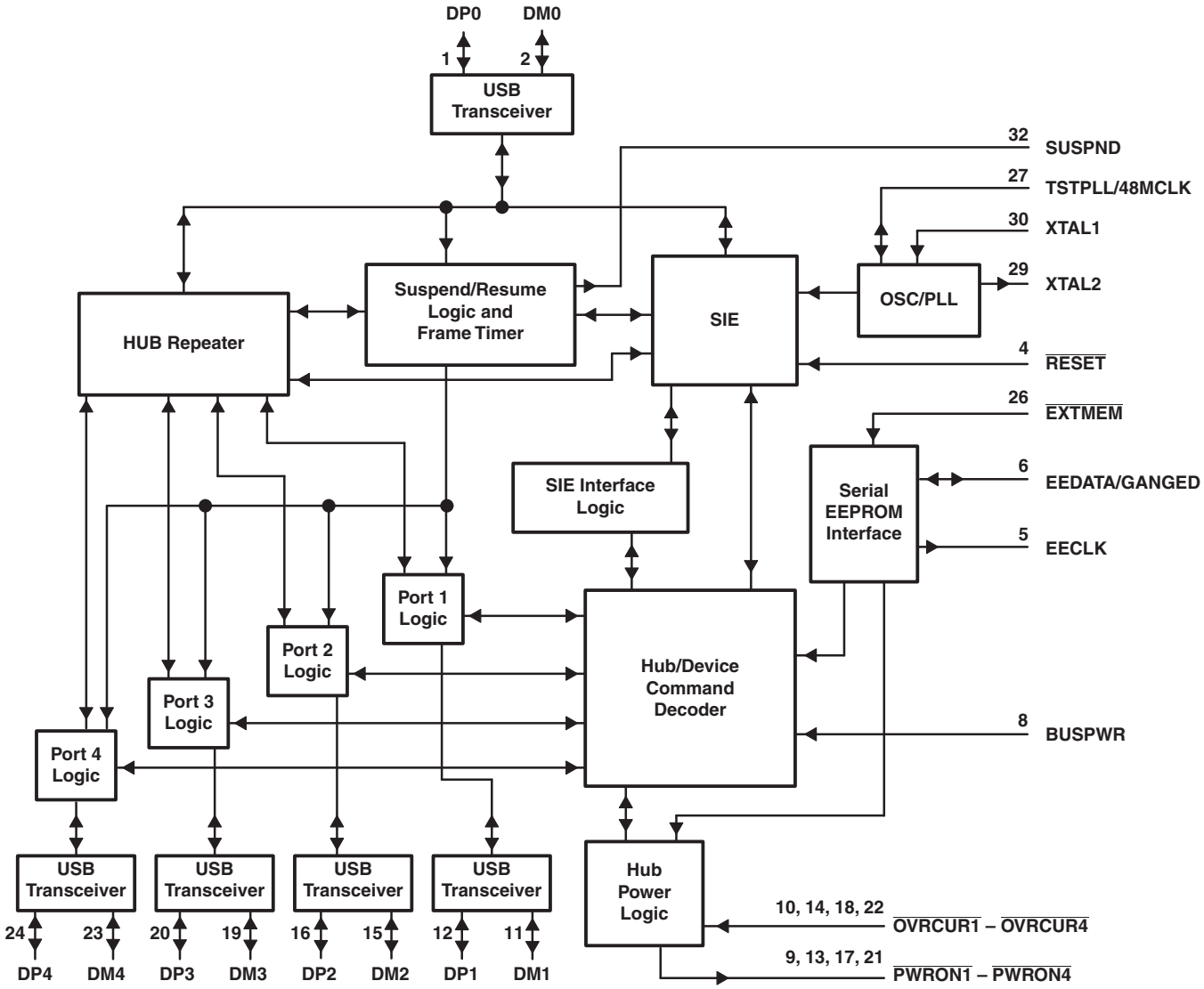
Figure 4. Differential Receiver Input Sensitivity Versus Common-Mode Input Range

8 Detailed Description

8.1 Overview

The TUSB2046BI-Q1 is a USB 2.0-compliant hub at full-speed as assigned by USB-IF TID #30220231. The device will enumerate high–speed devices, but limit the throughput to full–speed bit rates. The single upstream port and four downstream ports are equipped to support full-speed or low-speed connections. In the event of an overcurrent condition or failure, all or individual power pins can be configured to fail-safe open. A variety of clocking options allow the internal core of the device to be driven internally or externally with a crystal or resonator to achieve low EMI emission. The device contains an EEPROM controller for connection to an external EEPROM, which allows for automatic loading of static configuration data upon power-on reset, pin reset, or software reset. The EEPROM can be configured to load USB descriptors, USB device configuration, and the MAC address.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 USB Power Management

The TUSB2046BI-Q1 supports both bus-powered and self-powered modes. External power-management devices, such as the TPS2044, are required to control the 5-V power source switching (ON/OFF) to the downstream ports and to detect an overcurrent condition from the downstream ports individually or ganged. Outputs from external power devices provide overcurrent inputs to the TUSB2046BI-Q1 $\overline{\text{OVRCUR}}$ pins in case of an overcurrent condition, the corresponding $\overline{\text{PWRON}}$ pins are disabled by the TUSB2046BI-Q1. In the ganged mode, all $\overline{\text{PWRON}}$ signals transition simultaneously, and any $\overline{\text{OVRCUR}}$ input can be used. In the nonganged mode, the $\overline{\text{PWRON}}$ outputs and $\overline{\text{OVRCUR}}$ inputs operate on a per-port basis.

Both bus-powered and self-powered hubs require overcurrent protection for all downstream ports. The two types of protection are individual-port management (individual-port basis) or ganged-port management (multiple-port basis). Individual-port management requires power-management devices for each individual downstream port, but adds robustness to the USB system because, in the event of an overcurrent condition, the USB host only powers down the port that has the condition. The ganged configuration uses fewer power management devices and thus has lower system costs, but in the event of an overcurrent condition on any of the downstream ports, all the ganged ports are disabled by the USB host.

Using a combination of the $\overline{\text{BUSPWR}}$ and EEDATA/$\overline{\text{GANGED}}$ inputs, the TUSB2046BI-Q1 supports four modes of power management: bus-powered hub with either individual-port power management or ganged-port power management, and the self-powered hub with either individual-port power management or ganged-port power management. Texas Instruments supplies the complete hub solution because we offer this TUSB2046BI-Q1 along with the power-management devices needed to implement a fully USB compliant system.

8.3.2 Clock Generation

The TUSB2046BI-Q1 provides the flexibility of using either a 6-MHz or a 48-MHz clock. The logic level of the MODE pin controls the selection of the clock source. When MODE is low, the output of the internal APLL circuitry is selected to drive the internal core of the chip. When MODE is high, the XTAL1 input is selected as the input clock source and the APLL circuitry is powered down and bypassed. The internal oscillator cell is also powered down while MODE is high. For 6-MHz operation, TUSB2046BI-Q1 requires a 6-MHz clock signal on XTAL1 pin (with XTAL2 for a crystal) from which its internal APLL circuitry generates a 48-MHz internal clock to sample the data from the upstream port. For 48-MHz operation, the clock cannot be generated with a crystal, using the XTAL2 output, since the internal oscillator cell only supports the fundamental frequency. If low-power suspend and resume are desired, a passive crystal or resonator must be used, although the hub supports the flexibility of using any device that generates a 6-MHz clock. Because most oscillators cannot be stopped while power is on, their use prohibits low-power suspend, which depends on disabling the clock. When the oscillator is used, by connecting its output to the XTAL1 pin and leaving the XTAL2 pin open, its TTL output level cannot exceed 3.6 V. If a 6-MHz oscillator is used, it must be stopped at logic low whenever SUSPND is high. For crystal or resonator implementations, the XTAL1 pin is the input and the XTAL2 pin is used as the feedback path. A sample crystal tuning circuit is shown in Figure 8.

A sample crystal turning circuit is show in Figure 8.

8.4 Device Functional Modes

8.4.1 Vendor ID and Product ID With External Serial EEPROM

The $\overline{\text{EXTMEM}}$ enables or disables the optional EEPROM interface. When $\overline{\text{EXTMEM}}$ is high, the vendor and product IDs (VID and PID) use defaults, such that the message displayed during enumeration is General Purpose USB Hub. For this configuration, pin 6 functions as the GANGED input pin and the EECLK is unused. If custom VID and PID descriptors are desired, the $\overline{\text{EXTMEM}}$ must be tied low ($\overline{\text{EXTMEM}}$ = 0) and a SGS Thompson M93C46 EEPROM, or equivalent, stores the programmable VID, PID, and GANGED values. For this configuration, pins 5 and 6 function as the EEPROM interface signals with pin 5 as EECLK and pin 6 as EEDATA, respectively.

8.5 Programming

8.5.1 Programming the EEPROM

An SGS Thompson M93C46 EEPROM, or equivalent, stores the programmable VID and PID. When the EEPROM interface is enabled ($\overline{EXTMEM}$ = 0), the EECLK and EEDATA are internally pulled down (100 µA) inside the TUSB2046B-Q1. The internal pulldowns are disabled when the EEPROM interface is disabled ($\overline{EXTMEM}$ = 1).

The EEPROM is programmed with the three 16-bit locations as shown in Table 1. Connecting pin 6 of the EEPROM high (ORG = 1) organizes the EEPROM memory into 64×16-bit words.

Table 1. EEPROM Memory Map

ADDRESS	D15	D14	D13	D12–D8	D7–D0
00000	0	GANGED	00000	00000	00000000
00001	VID high-byte				VID low-byte
00010	PID high-byte				PID low-byte
	XXXXXXXX				

The D and Q signals of the EEPROM must be tied together using a 1-kΩ resistor with the common I/O operations forming a single-wire bus. After system power-on reset, the TUSB2046B-Q1 performs a one-time access read operation from the EEPROM if the $\overline{EXTMEM}$ pin is pulled low and the chip select(s) of the EEPROM is connected to the system power-on reset. Initially, the EEDATA pin is driven by the TUSB2046B-Q1 to send a start bit (1) which is followed by the read instruction (10) and the starting-word address (00000). Once the read instruction is received, the instruction and address are decoded by the EEPROM, which then sends the data to the output shift register. At this point, the hub stops driving the EEDATA pin and the EEPROM starts driving. A dummy (0) bit is then output and the first three 16-bit words in the EEPROM are output with the most significant bit (MSB) first.

The output data changes are triggered by the rising edge of the clock provided by the TUSB2046B-Q1 on the EECLK pin. The SGS-Thompson M936C46 EEPROM is recommended because it advances to the next memory location by automatically incrementing the address internally. Any EEPROM used must have the automatic internal address advance function. After reading the three words of data from the EEPROM, the TUSB2046B-Q1 puts the EEPROM interface into a high-impedance condition (pulled down internally) to allow other logic to share the EEPROM. The EEPROM read operation is summarized in Figure 5. For more details on EEPROM operation, refer to *SGS-Thompson Microelectronics M93C46 Serial Microwire Bus EEPROM* data sheet.

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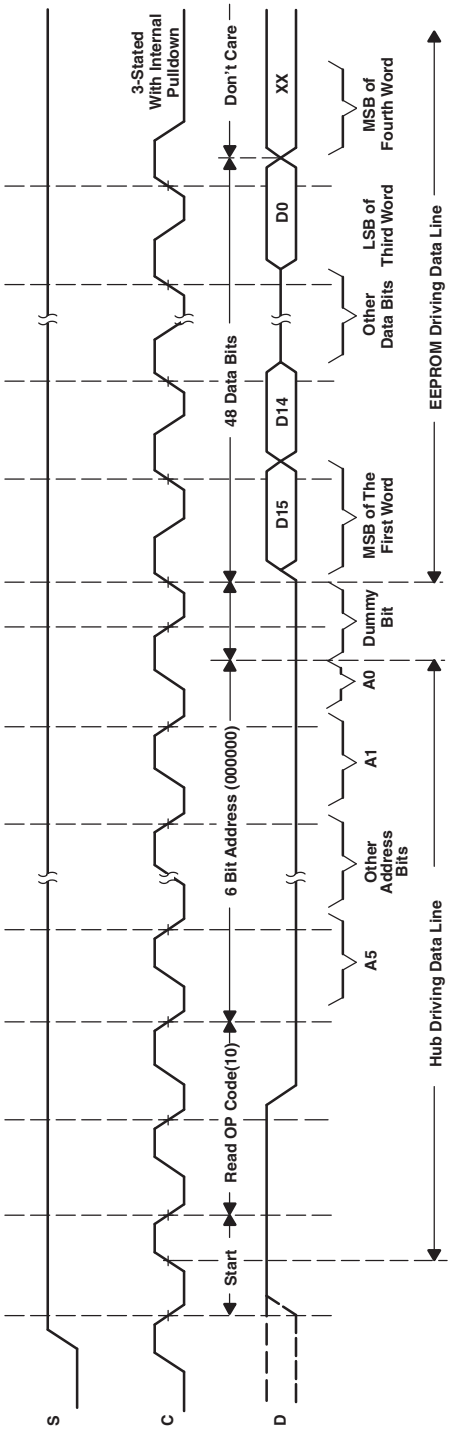

Figure 5. EEPROM Read Operation Timing Diagram

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Another advantage of USB is that all peripherals are connected using a standardized four-wire cable that provides both communication and power distribution. The power configurations are bus-powered and self-powered modes. The maximum current that may be drawn from the USB 5-V line during power up is 100 mA. For the bus-powered mode, a hub can draw a maximum of 500 mA from the 5-V line of the USB cable. A bus-powered hub must always be connected downstream to a self-powered hub unless it is the only hub connected to the PC and there are no high-powered functions connected downstream. In the self-powered mode, the hub is connected to an external power supply and can supply up to 500 mA to each downstream port. High-powered functions may draw a maximum of 500 mA from each downstream port and may only be connected downstream to self-powered hubs. Per the USB specification, in the bus-powered mode, each downstream port can provide a maximum of 100 mA of current, and in the self-powered mode, each downstream port can provide a maximum of 500 mA of current.

Both bus-powered and self-powered hubs require overcurrent protection for all downstream ports. The two types of protection are individual-port management (individual-port basis) or ganged-port management (multiple-port basis). Individual-port management requires power-management devices for each individual downstream port, but adds robustness to the USB system because, in the event of an overcurrent condition, the USB host only powers down the port that has the condition. The ganged configuration uses fewer power management devices and thus has lower system costs, but in the event of an overcurrent condition on any of the downstream ports, all the ganged ports are disabled by the USB host.

Using a combination of the BUSPWR and EEDATA/GANGED inputs, the TUSB2046B-Q1 supports four modes of power management: bus-powered hub with either individual-port power management or ganged-port power management, and the self-powered hub with either individual-port power management or ganged-port power management. Texas Instruments supplies the complete hub solution with the TUSB2036 (2/3-port), TUSB2046B-Q1, and the TUSB2077 (7-port) hubs along with the power-management devices needed to implement a fully USB specification-compliant system.

A major advantage of USB is the ability to connect 127 functions configured in up to 6 logical layers (tiers) to a single personal computer (see Figure 6).

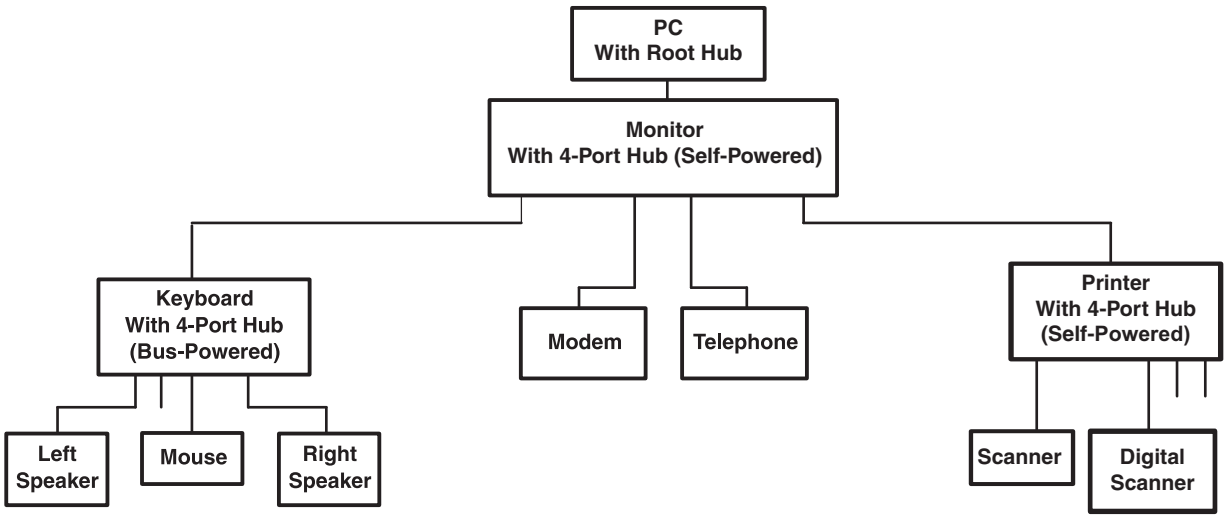

Figure 6. USB-Tiered Configuration Example

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Application Information (continued)

9.1.1 Input Clock Configuration

The input clock configuration logic of TUSB2046B-Q1 is enhanced to accept a 6-MHz crystal or 48-MHz on-the-board clock source with a simple tie-off change on TSTMODE (pin 31).

- A 6-MHz input clock configuration is shown in Figure 7.
  In this mode, both the TSTMODE and TSTPLL/48MCLK pins must be tied to ground. The hub is configured to use the 6-MHz clock on pins 30 and 29, which are XTAL1 and XTAL2, respectively, on the TUSB2046B-Q1. This is identical to the TUSB2046.

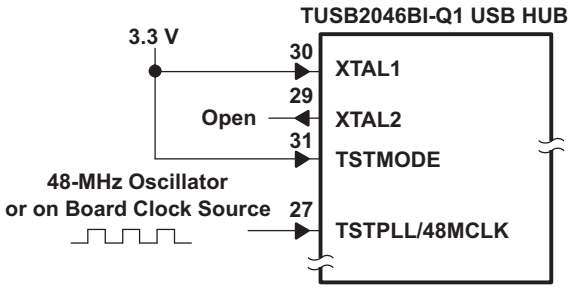
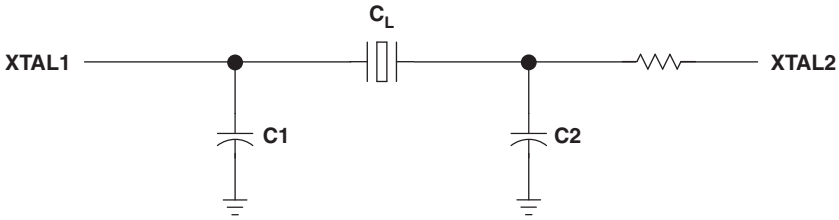


Figure 7. 6-MHz Input Clock Configuration

Figure 8 is an example of how to generate the 6-MHz clock signal.



NOTE: This figure assumes a 6-MHz fundamental crystal that is parallel loaded. The component values of C1, C2, and R_d are determined using a Fox Electronics part number HC49U-6.00MHz 30\50\0-70\20 crystal or equivalent, which means ±30 ppm at 25°C and ±50 ppm from 0°C to 70°C. The characteristics for the crystal include a load capacitance (C_L) of 20 pF, maximum shunt capacitance (C_o) of 7 pF, and the maximum ESR of 50 Ω. In order to ensure enough negative resistance, use C1 = C2 = 27 pF. The resistor R_d is used to trim the gain, and R_d = 1.5 kΩ is recommended.

Figure 8. Crystal Tuning Circuit

- A 48-MHz input clock configuration is shown in Figure 9.
  In this mode, both TSTMODE and XTAL1 pins must be tied to 3.3-V V_{CC}. The hub accepts the 48-MHz clock input on TSTPLL/48MCLK (pin 27). XTAL2 must be left floating (open) for this configuration. Only the oscillator or the onboard clock source is accepted for this mode. A crystal can not be used for this mode, since the chip's internal oscillator cell only supports the fundamental frequency.

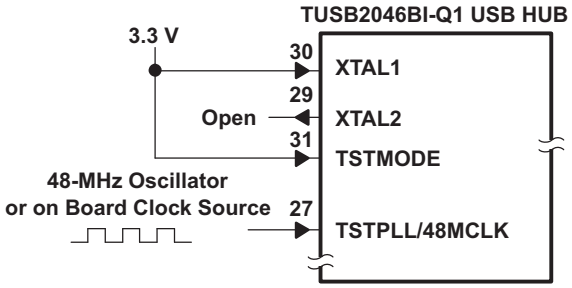


Figure 9. 48-MHz Input Clock Configuration

Application Information (continued)

Figure 10 is a block diagram example of how to connect the external EEPROM if a custom product ID and vendor ID are desired. Figure 5 shows the EEPROM read operation timing diagram. Figure 13, Figure 14, and Figure 11 illustrate how to connect the TUSB2046B-Q1 device for different power source and port power-management combinations.

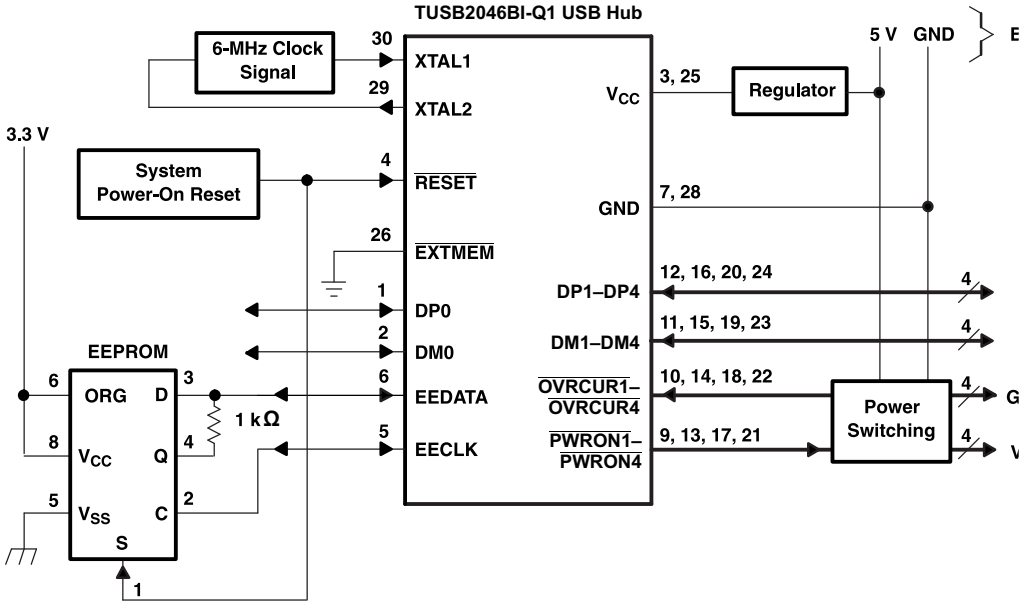


Figure 10. Typical Application of the TUSB2046B-Q1 USB Hub

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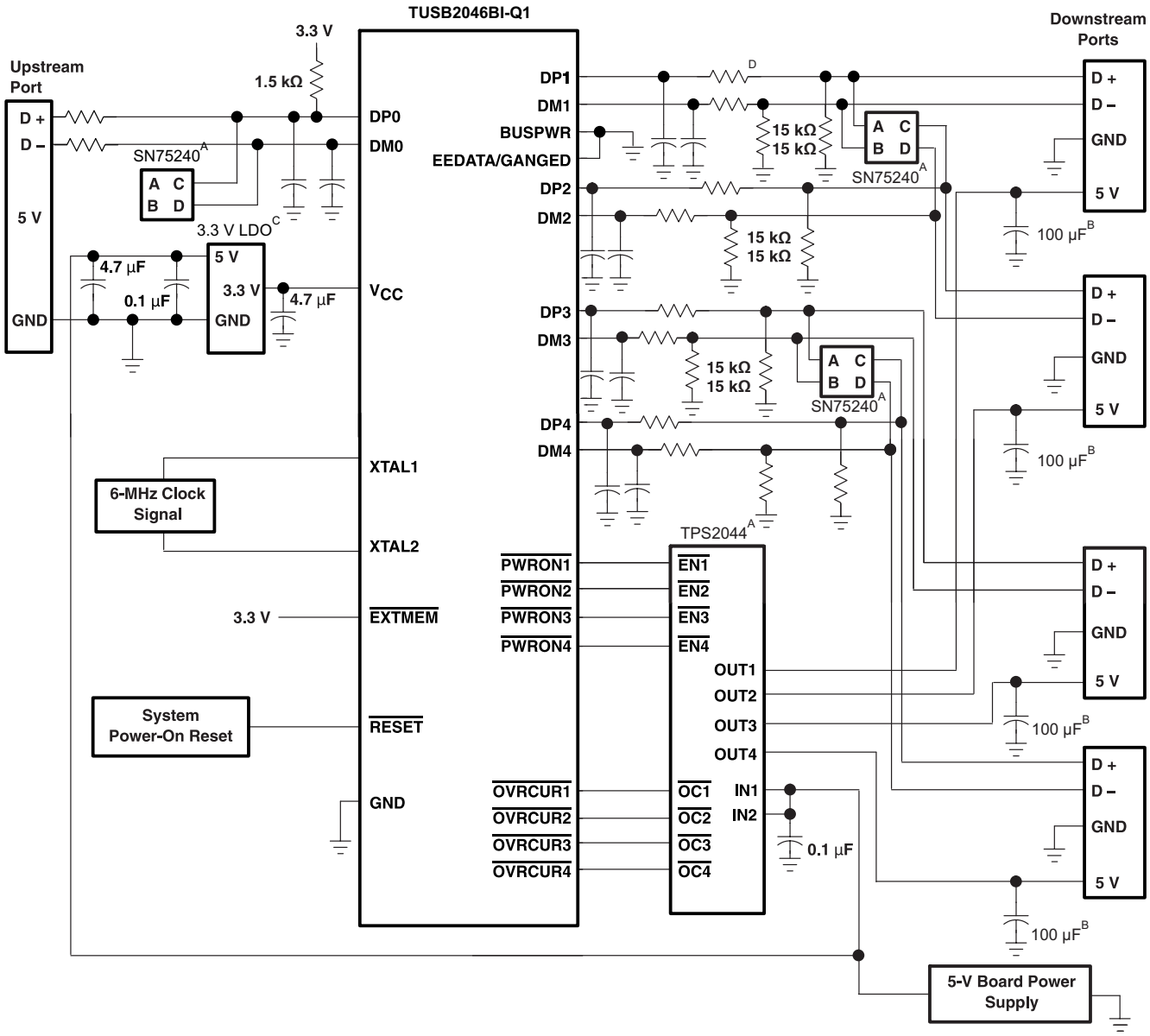
9.2 Typical Applications

9.2.1 Self-Powered Hub, Individual-Port Power Management



NOTES: A. TPS2044, TPS2042, and SN75240 are Texas Instruments devices. Two TPS2042 devices can be substituted for the TPS2044. The $\overline{\text{OCn}}$ outputs of the TPS204n are open-drain. A 10-kΩ pullup is recommended.
B. 120 µF per hub is the minimum required per the USB specification. However, TI recommends a 100-µF, low-ESR, tantalum capacitor per port for immunity to voltage droop.
C. LDO is a 5-V-to-3.3-V voltage regulator.
D. All USB DP, DM signal pairs require series resistors of approximately 27Ω to ensure proper termination. An optional filter capacitor of about 22 pF is recommended for EMI suppression. This capacitor, if used, must be placed between the hub terminal and the series resistor, as per section 7.1.6 of the USB specification.

Figure 11. TUSB2046B-Q1 Self-Powered Hub, Individual-Port Power-Management Application

9.2.1.1 Design Requirements

For this example, follow the design parameters listed in Table 2.

Typical Applications (continued)

Table 2. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
VCC Supply	3.3 V
Downstream Ports	4
Power Management	Individual-Port
Clock Source	6-MHz Crystal
External EEPROM	No
Power Source Mode	Self-Powered

9.2.1.2 Detailed Design Procedure

In a self-powered configuration, the TUSB2046-Q1 can be implemented for individual-port power management when used with the TPS2044, because it can supply 500 mA of current to each downstream port, and can provide current limiting on a per-port basis. When the hub detects a fault on a downstream port, power is removed from the port with the fault; the remaining ports continue to operate normally. Self-powered hubs are required to implement overcurrent protection and report overcurrent conditions. The SN75240 transient suppressors reduce inrush current and voltage spikes on the data lines.

9.2.1.3 Application Curve

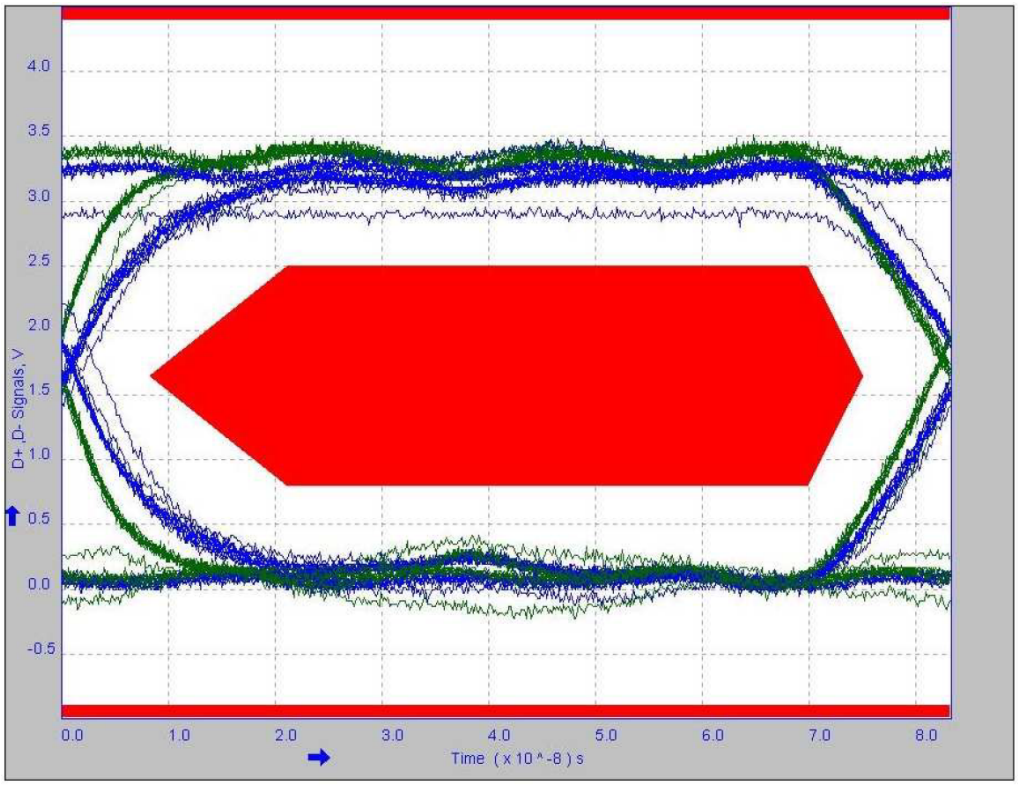


Figure 12. Downstream Port 1

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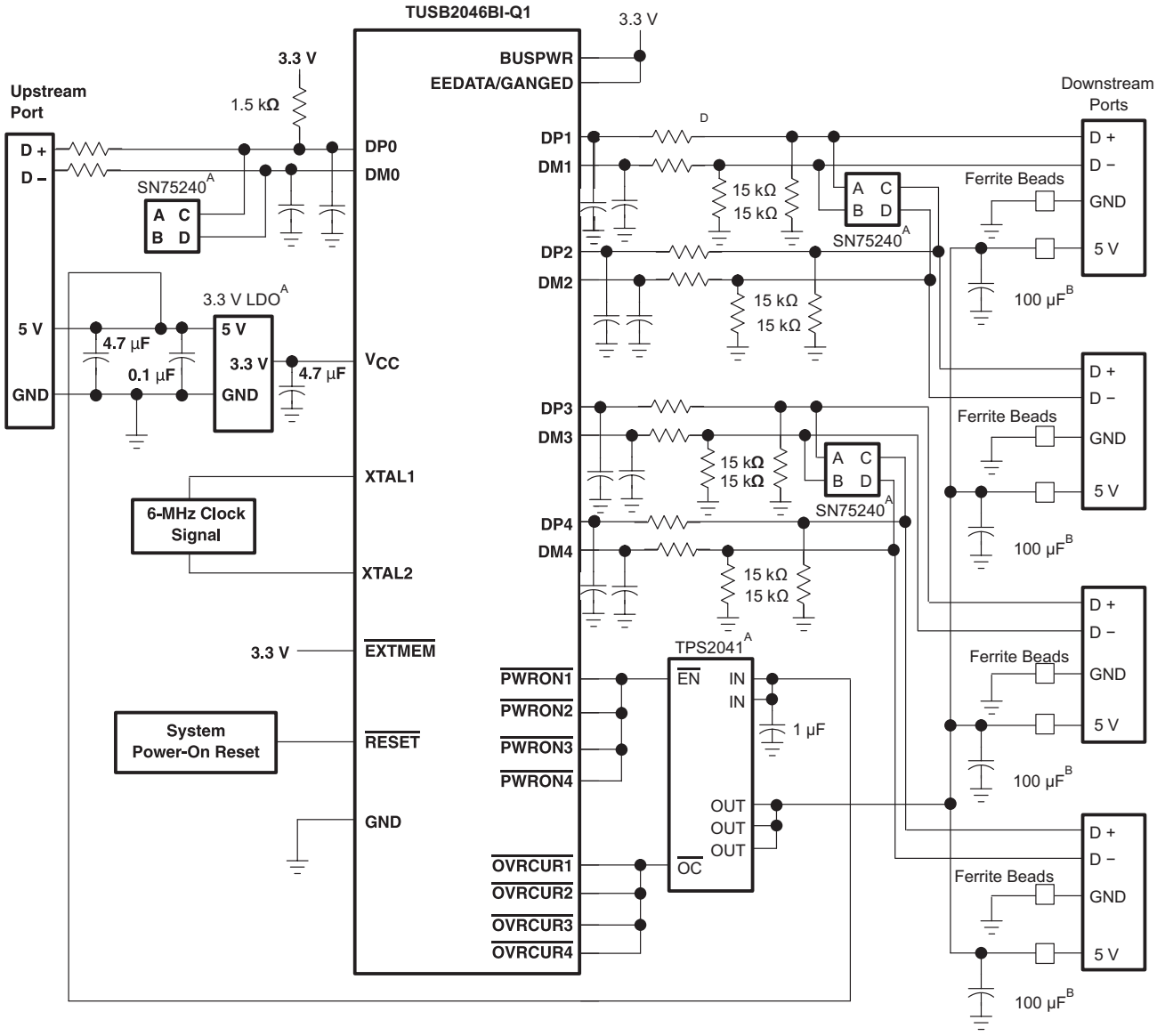
9.2.2 Bus-Powered Hub, Ganged-Port Power Management

When used in bus-powered mode, the TUSB2046B-Q1 supports up to four downstream ports by controlling a TPS2041 device which is capable of supplying 100 mA of current to each downstream port. Bus-powered hubs must implement power switching to ensure current demand is held below 100 mA when the hub is hot-plugged into the system. Utilizing the TPS2041 for ganged-port power management provides overcurrent protection for the downstream ports. The SN75240 transient suppressors reduce inrush current and voltage spikes on the data lines. The $\overline{\text{OVRCUR}}$ signals must be tied together for a ganged operation.



NOTES: A. TPS2041 and SN75240 are Texas Instruments devices. The $\overline{\text{OCn}}$ outputs of the TPS204n are open-drain. A 10-kΩ pullup is recommended.
B. 120 µF per hub is the minimum required per the USB specification. However, TI recommends a 100-µF, low-ESR, tantalum capacitor per port for immunity to voltage droop.
C. LDO is a 5-V-to-3.3-V voltage regulator
D. All USB DP, DM signal pairs require series resistors of approximately 27 Ω to ensure proper termination. An optional filter capacitor of about 22 pF is recommended for EMI suppression. This capacitor, if used, must be placed between the hub terminal and the series resistor, as per section 7.1.6 of the USB specification.

Figure 13. TUSB2046B-Q1 Bus-Powered Hub, Ganged-Port Power-Management Application

9.2.2.1 Design Requirements

Table 3 lists the design parameters for this example.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VCC Supply	3.3 V
Downstream Ports	4
Power Management	Individual-Port
Clock Source	6-MHz Crystal
External EEPROM	No
Power Source Mod	Self-Powered

9.2.2.2 Detailed Design Procedures

In a self-powered configuration, the TUSB2046-Q1 can be implemented for individual-port power management when used with the TPS2044 because it is capable of supplying 500 mA of current to each downstream port and can provide current limiting on a per-port basis. When the hub detects a fault on a downstream port, power is removed from only the port with the fault and the remaining ports continue to operate normally. Self-powered hubs are required to implement overcurrent protection and report overcurrent conditions. The SN75240 transient suppressors reduce inrush current and voltage spikes on the data lines.

9.2.3 Self-Powered Hub, Ganged-Port Power Management

The TUSB2046B-Q1 can also be implemented for ganged-port power management in a self-powered configuration. The implementation is very similar to the bus-powered example with the exception that a self-powered port supplies 500 mA of current to each downstream port. The overcurrent protection can be provided by a TPS2044 quad device or a TPS2024 single power switch.

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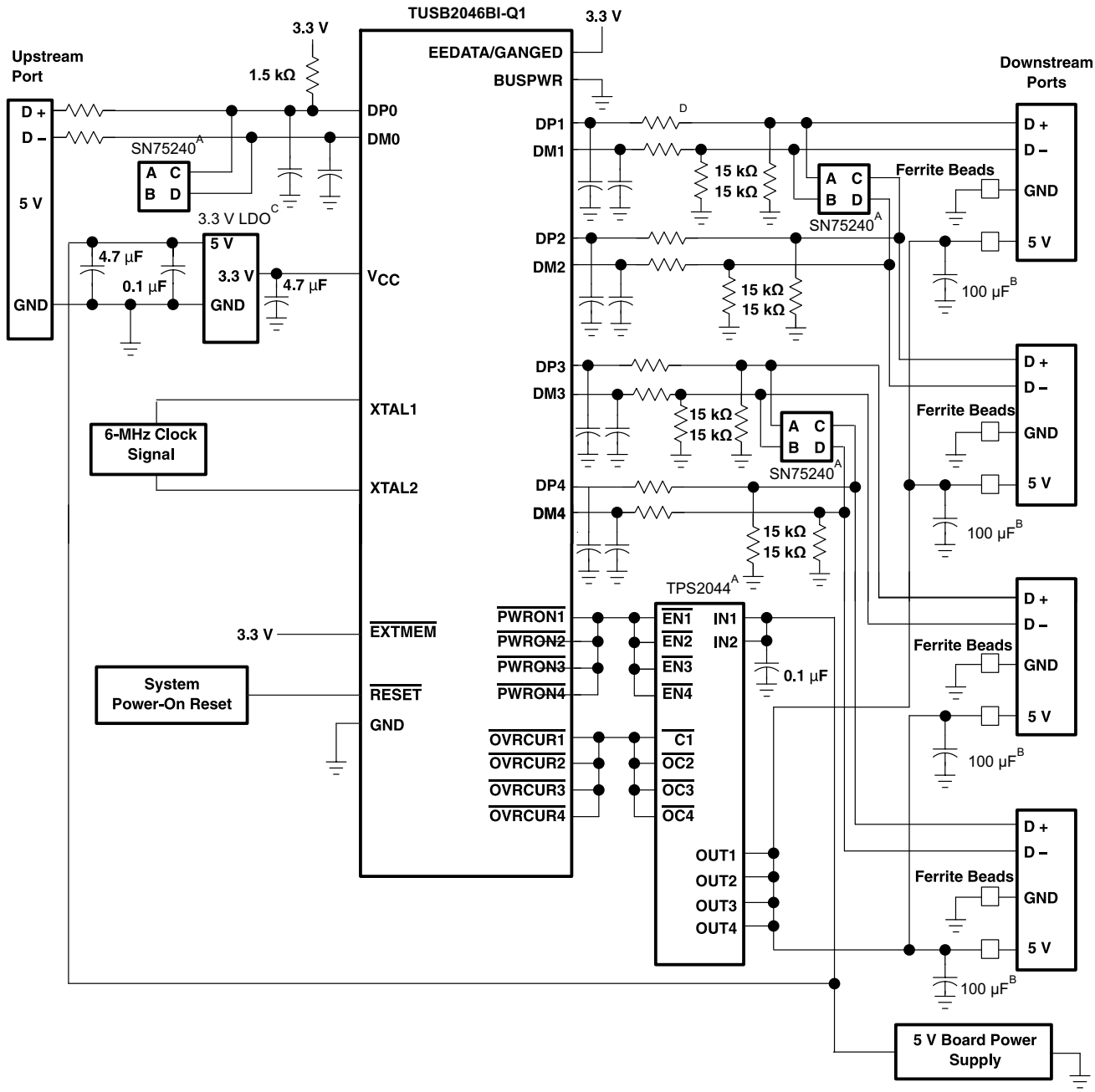

NOTES: A. TPS2044, TPS2042, and SN75240 are Texas Instruments devices. The TPS2042 can be substituted for the TPS2044. The $\overline{OCn}$ outputs of the TPS204n are open-drain. A 10-kΩ pullup is recommended.
B. 120 µF per hub is the minimum required per the USB specification. However, TI recommends a 100-µF, low-ESR, tantalum capacitor per port for immunity to voltage droop.
C. LDO is a 5-V-to-3.3-V voltage regulator.
D. All USB DP, DM signal pairs require series resistors of approximately 27Ω to ensure proper termination. An optional filter capacitor of about 22 pF is recommended for EMI suppression. This capacitor, if used, must be placed between the hub terminal and the series resistor, as per section 7.1.6 of the USB specification.

Figure 14. TUSB2046B-Q1 Self-Powered Hub, Ganged-Port Power-Management Application

10 Power Supply Recommendations

10.1 TUSB2046BI-Q1 Power Supply

V_{CC} should be implemented as a single power plane.

- The V_{CC} pins of the TUSB2046B-Q1 supply 3.3-V power rail to the I/O of the TUSB2046B-Q1. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- All power rails require a 10-µF capacitor or 1-µF capacitors for stability and noise immunity. These bulk capacitors can be placed anywhere on the power rail. The smaller decoupling capacitors should be placed as close to the TUSB2046BI-Q1 power pins as possible with an optimal grouping of two of differing values per pin.

10.2 Downstream Port Power

- The downstream port power, VBUS, must be supplied by a source capable of supplying 5 V and up to 500 mA per port. Downstream port power switches can be controlled by the TUSB2046B-Q1 signals. It is also possible to leave the downstream port power always enabled.
- A large bulk low-ESR capacitor of 22 µF or larger is required on each downstream port's VBUS to limit in-rush current.
- The ferrite beads on the VBUS pins of the downstream USB port connections are recommended for both ESD and EMI reasons. A 0.1-µF capacitor on the USB connector side of the ferrite provides a low impedance path to ground for fast rise time ESD current that might have coupled onto the VBUS trace from the cable.

11 Layout

11.1 Layout Guidelines

11.1.1 Placement

1. A 0.1 µF should be placed as close as possible on VCC power pin.
2. The ESD and EMI protection devices (if used) should also be placed as possible to the USB connector.
3. If a crystal is used, it must be placed as close as possible to the TUSB2046-Q1's XTAL1 and XTAL2 pins.
4. Place voltage regulators as far away as possible from the TUSB2046-Q1, the crystal, and the differential pairs.
5. In general, the large bulk capacitors associated with the power rail should be placed as close as possible to the voltage regulators.

11.1.2 Differential Pairs

1. Must be designed with a differential impedance of 90 Ω ±10%.
2. Route all differential pairs on the same layer adjacent to a solid ground plane.
3. Do not route differential pairs over any plane split.
4. Adding test points will cause impedance discontinuity and will therefore negative impact signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes stub on the differential pair.
5. Avoid 90 degree turns in trace. The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥ 135 degrees. This will minimize any length mismatch causes by the bends and therefore minimize the impact bends have on EMI.
6. Minimize the trace lengths of the differential pair traces. The maximum recommended trace length for USB 2.0 differential pair signals is eight inches. Longer trace lengths require very careful routing to assure proper signal integrity.
7. Match the etch lengths of the differential pair traces. The USB 2.0 differential pairs should not exceed 50 mils relative trace length difference.

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Layout Guidelines (continued)

8. Minimize the use of vias in the differential pair paths as much as possible. If this is not practical, make sure that the same via type and placement are used for both signals in a pair. Any vias used should be placed as close as possible to the TUSB2046-Q1 device.
9. Do not place power fuses across the differential pair traces.

11.1.3 Ground

TI recommends using only one board ground plane in the design. This provides the best image plane for signal traces running above the plane. The thermal pad of the TUSB2046-Q1 and any of the voltage regulators should be connected to this plane with vias. An earth or chassis ground is implemented only near the USB port connectors on a different plane for EMI and ESD purposes.

11.2 Layout Example

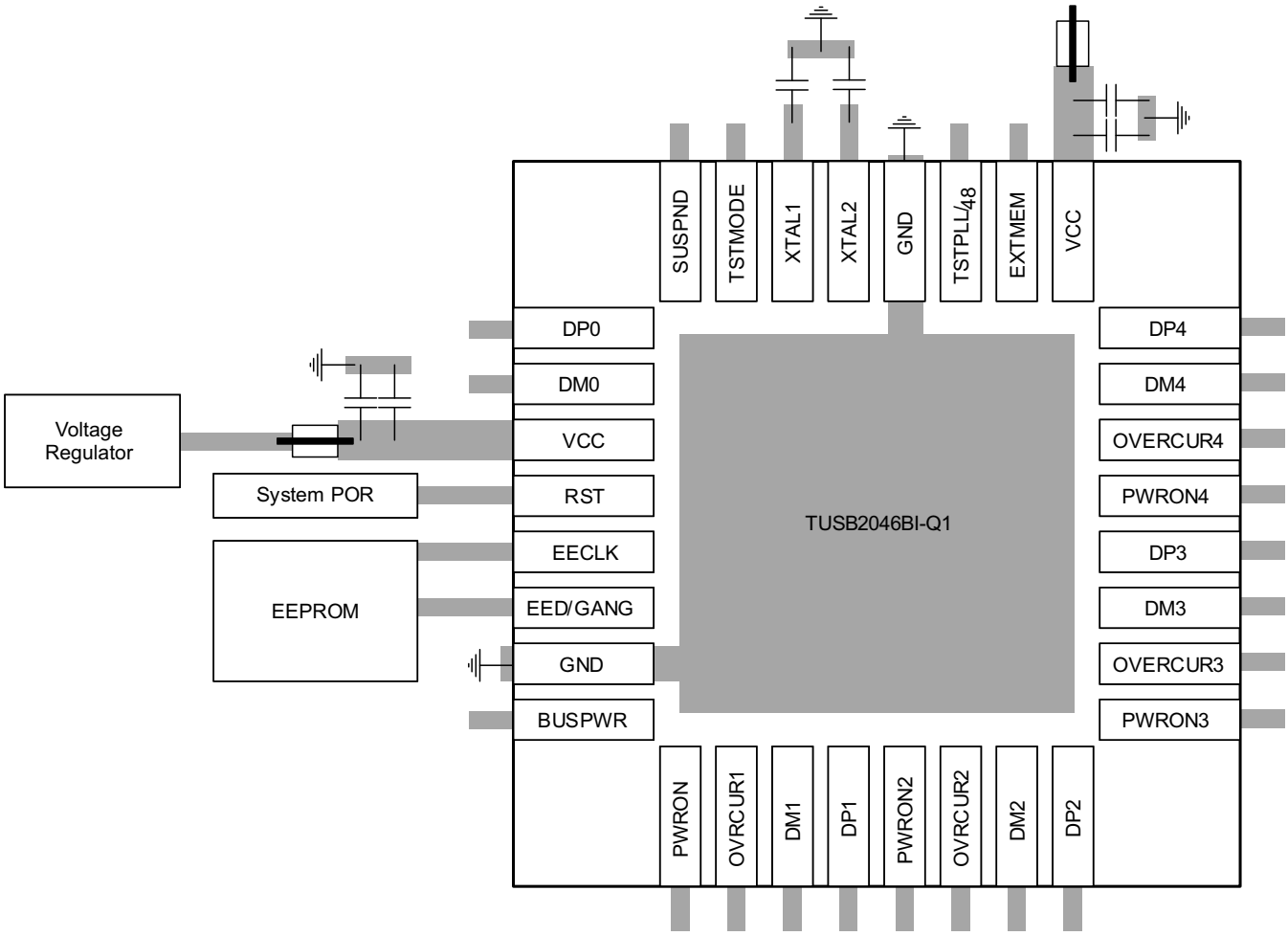

Figure 15. Layout Example

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB2046BIRHBRQ1	OBSOLETE	VQFN	RHB	32		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TUSB 2046BQ1	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TUSB2046B-Q1 :

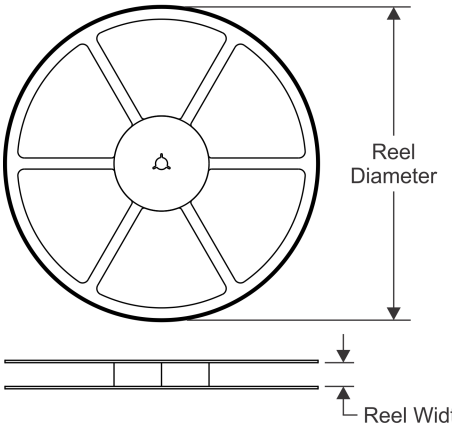
- Catalog: TUSB2046B

NOTE: Qualified Version Definitions:

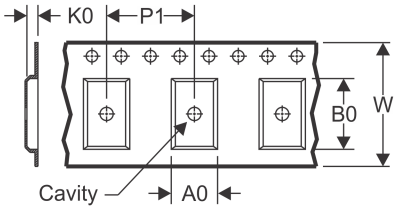
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

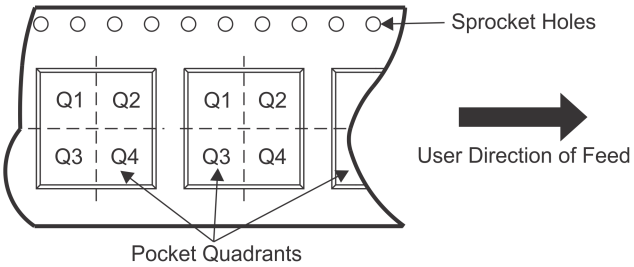


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

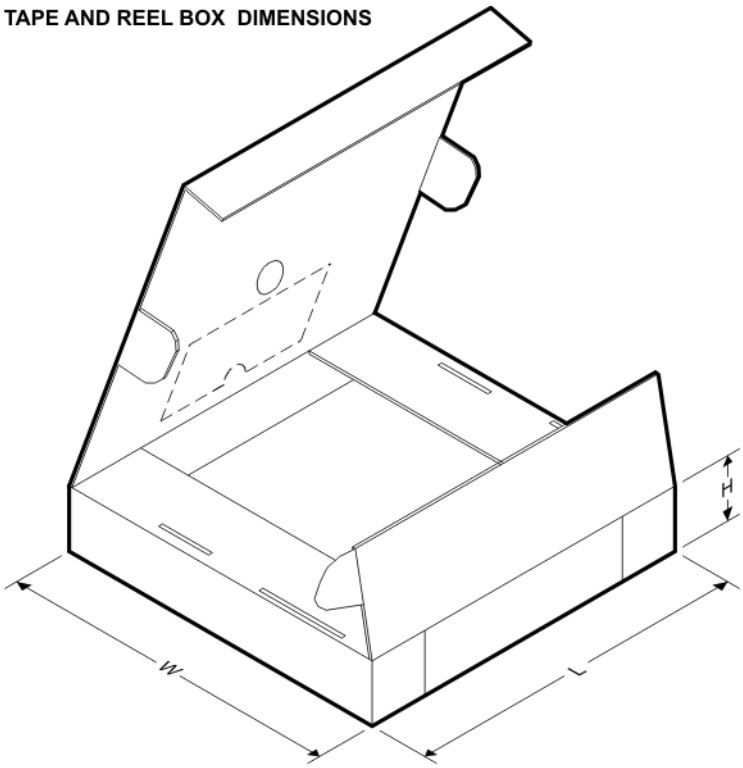
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB2046BIRHBRQ1	VQFN	RHB	32	0	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

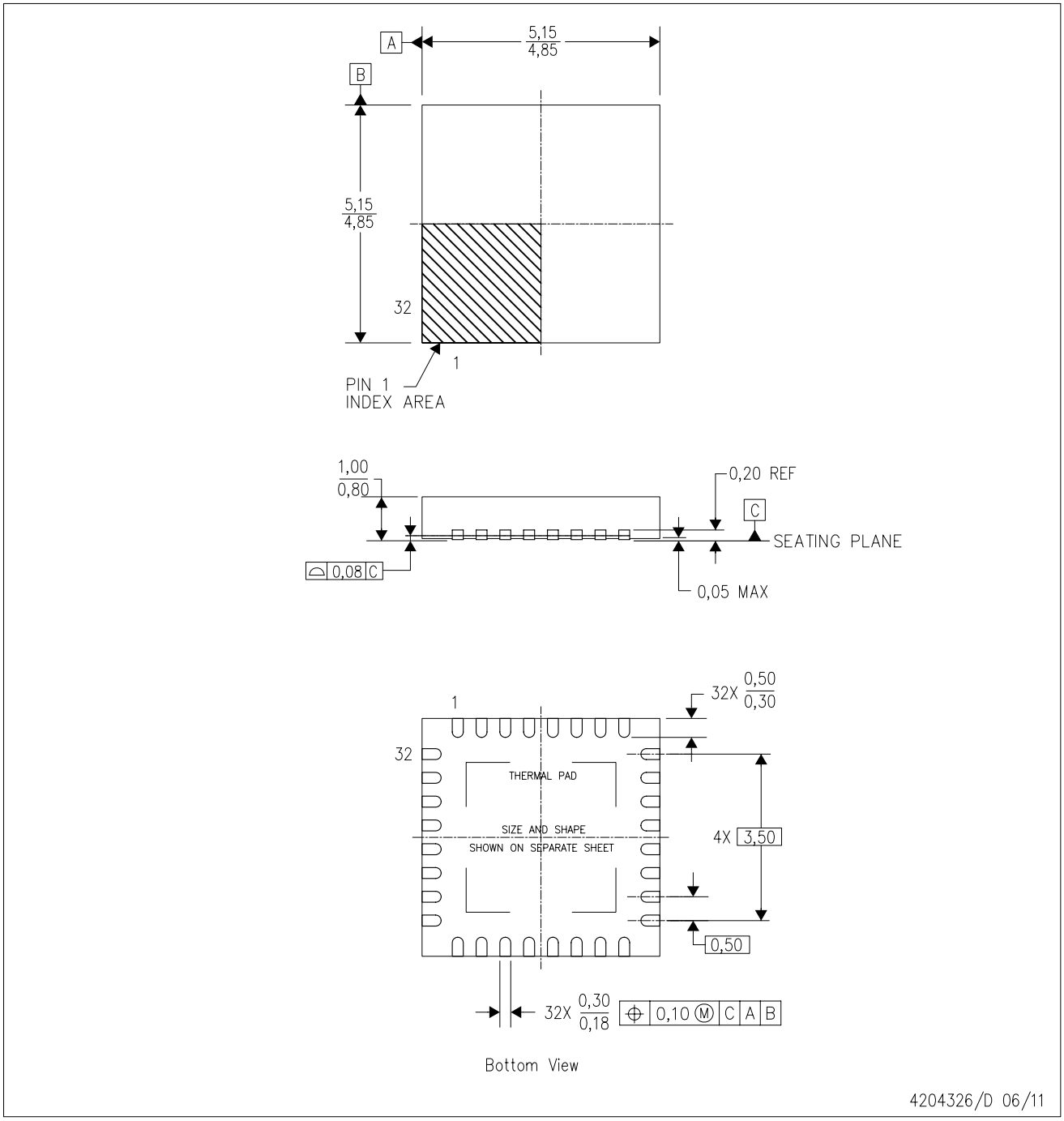
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB2046BIRHBRQ1	VQFN	RHB	32	0	338.1	338.1	20.6

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

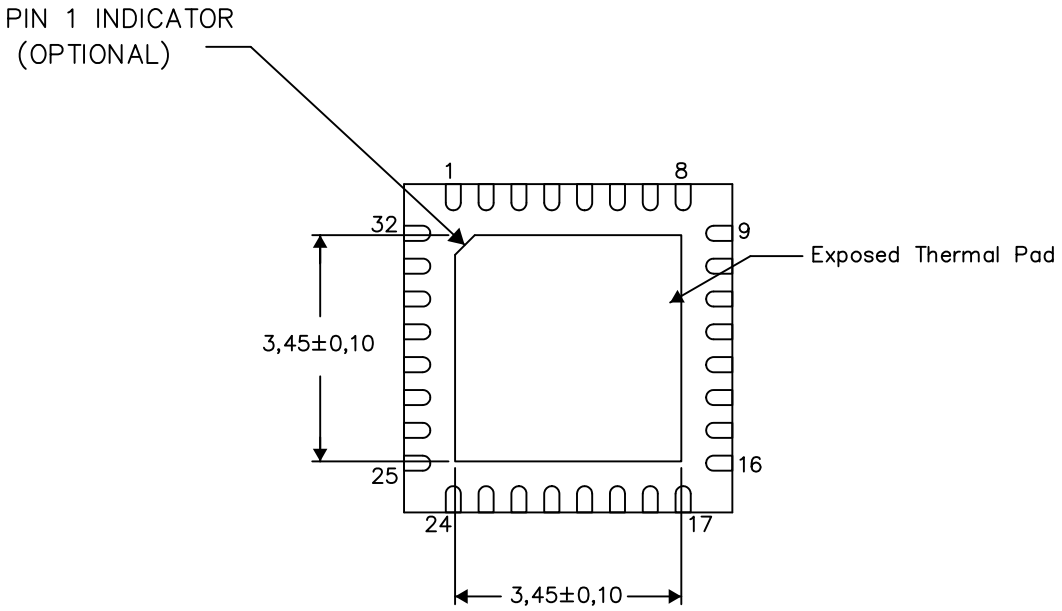
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



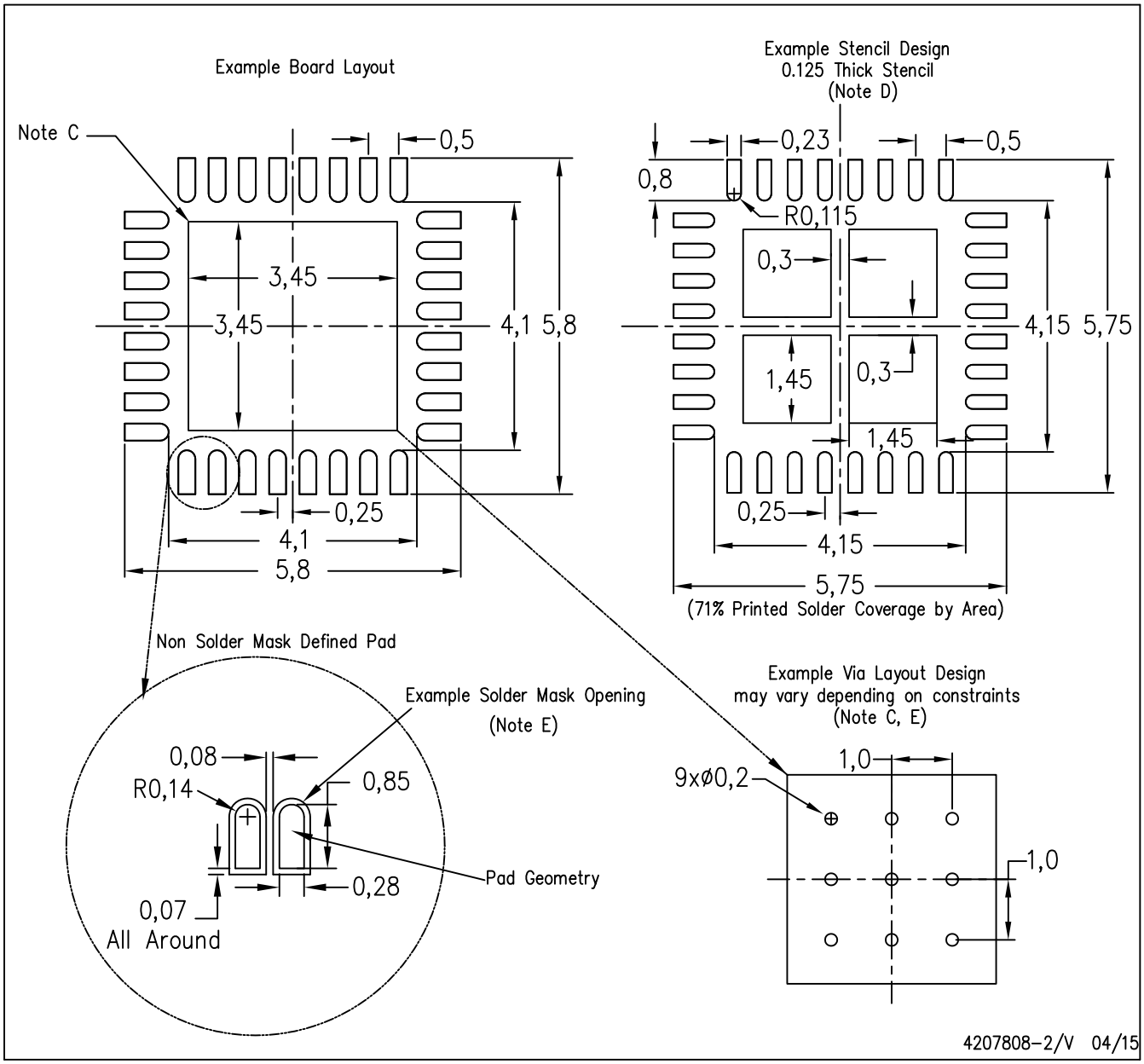
Bottom View

Exposed Thermal Pad Dimensions

4206356–2/AC 05/15

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

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